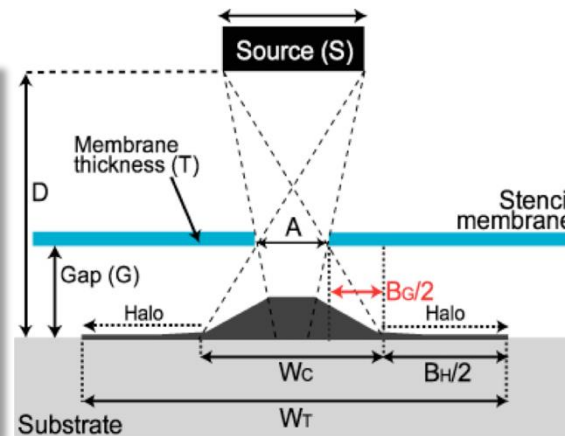
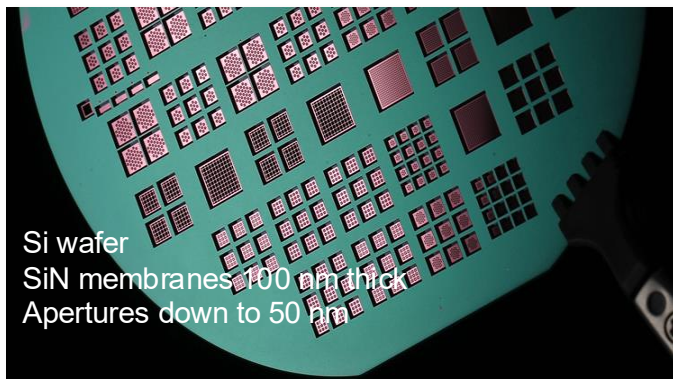
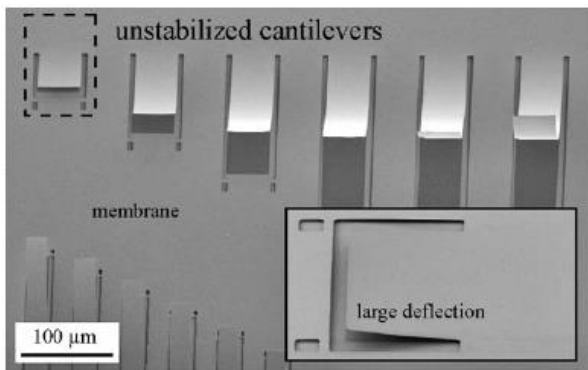


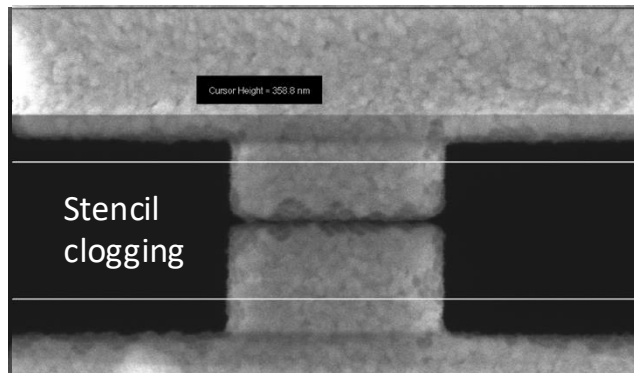
Nanostenciling



Problem: stress / bending



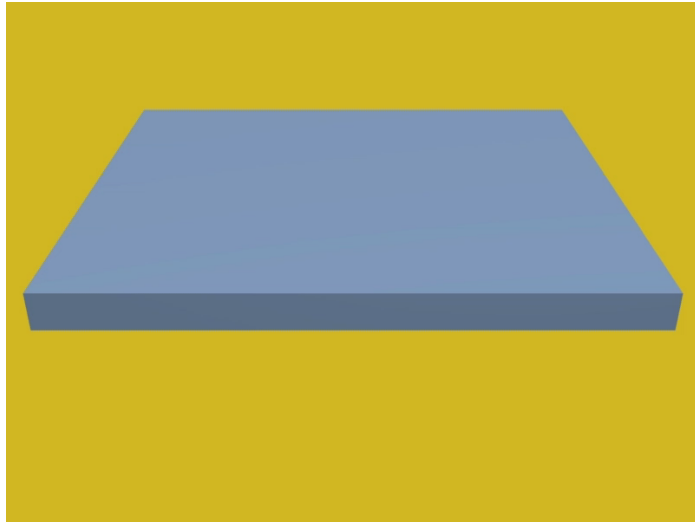
Problem: clogging



- Short recap on lithography resolution and lift-off on the blackboard
- Stencil lithography: basics and advanced
- T-SPL lithography: basics and advanced

Stencil lithography

- High resolution shadow masks
- Simple application examples
- Unique configurations where ordinary lithography would fail
- Blurring and diffusion issues
- Dynamic stencil



Prof. Oscar
Vazquez-Mena
UC San Diego

Nanostencil lithography

Many challenges:

Gap

Blurring

Membrane stability

Alignment

But also many opportunities:

Vacuum clean

No resist chemistry

Fast and simple, cost efficient nano

Wide choice of material & substrates

Mainly for PVD

Contents lists available at [ScienceDirect](#)

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

ELSEVIER

MECH-ELECTRONIC ENGINEERING

Review Article

Resistless nanofabrication by stencil lithography: A review

O. Vazquez-Mena^{a,*}, L. Gross^b, S. Xie^a, L.G. Villanueva^a, J. Brugger^{a,*}

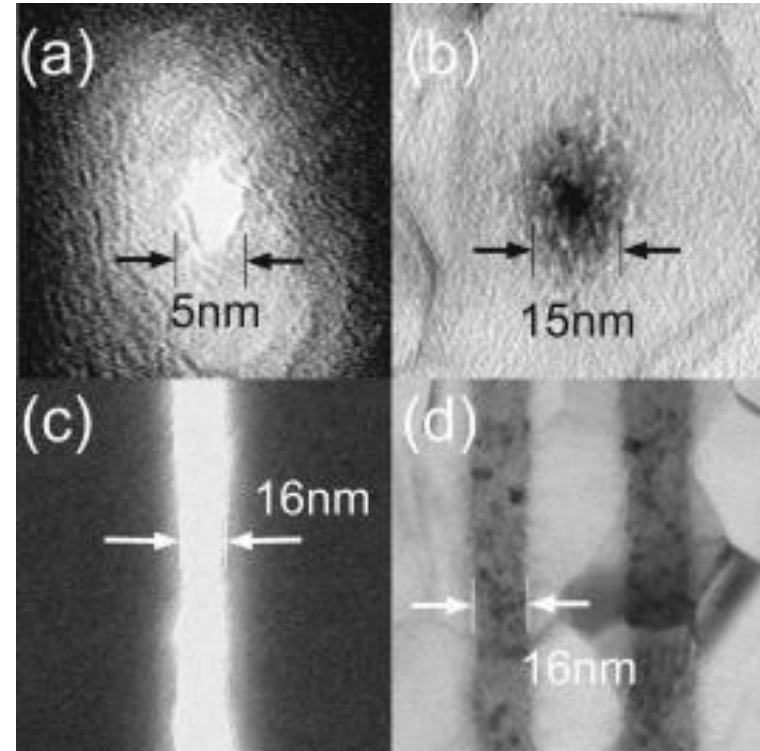
^a Microsystems Laboratory, Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
^b IBM Research – Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

CrossMark

Nanostenciling (1999)

Bright-field STEM images. (a) A hole 5 nm in diameter etched through a silicon nitride membrane. (b) A metal dot made by evaporating 10 nm of Er through an orifice 5–10 nm in diameter onto an oxidized aluminum film held at room temperature. (c) Section of a $4\ \mu\text{m}$ -long \times 15–20-nm-wide line etched through a silicon nitride membrane. (d) Sections of 10-nm-thick Er lines which are deposited through an orifice similar to the one shown in (c), at room temperature onto an oxidized Al film. The two lines, 19 nm and 16 nm wide, were made by separate depositions of Er, from different angles, through the same linear hole

Early works and probably world record



Deshmukh et al APL 1999

Stencil fabrication

LPCVD 50-500 nm thick SiN

Pattern definition in photoresist

Pattern transfer into SiN

Membrane window definition and KOH etching

Fabrication of nanoscale apertures in membrane by:

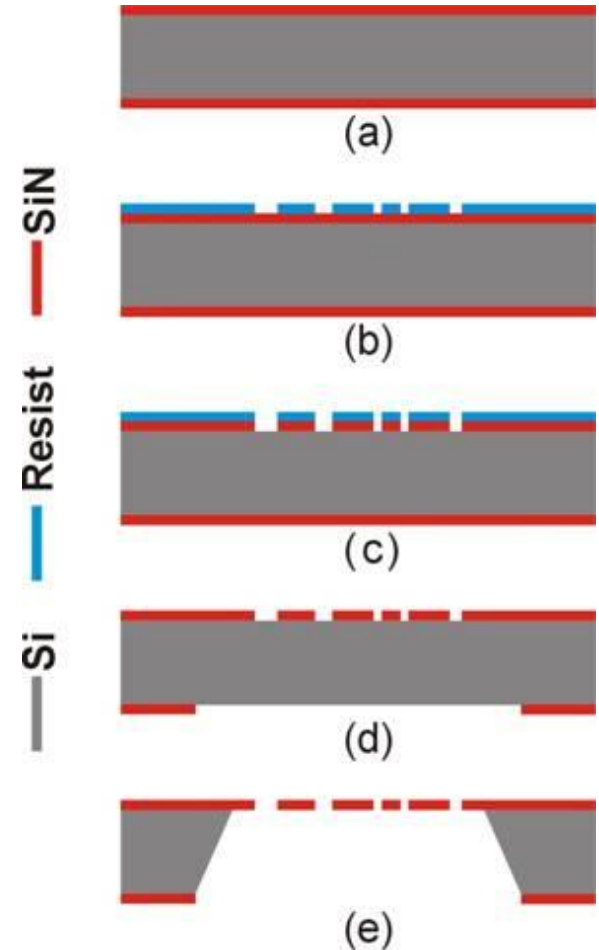
- Focused Ion Beam Milling

- Electron beam lithography

- Laser interference lithography

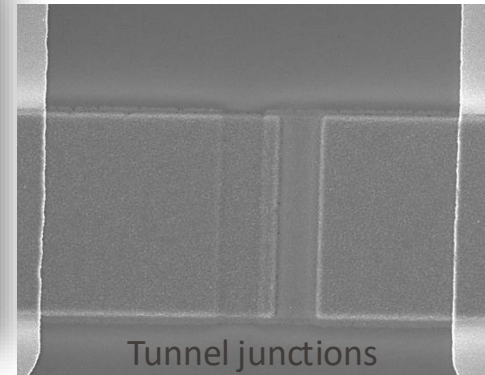
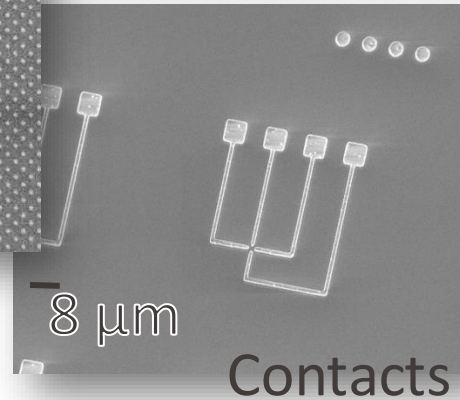
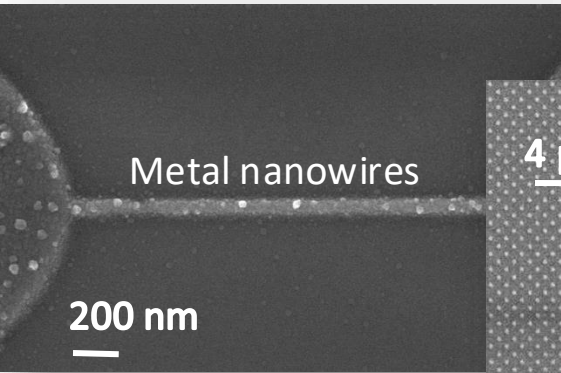
- Nanoimprint lithography

- Deep UV lithography



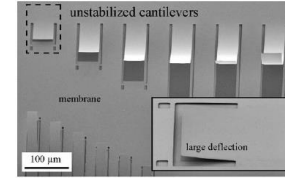
What can be done?

- Deposition of different metals
 - Aluminium, Gold, Chromium, Titanium, Platinum, etc.
- Metallic structures

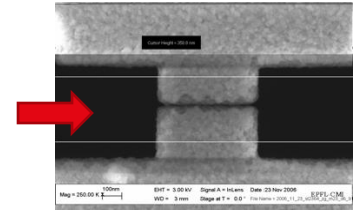
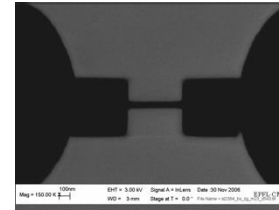


Major challenges

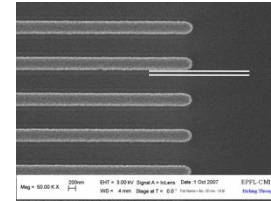
Membrane stability



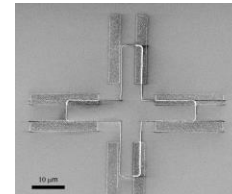
Clogging



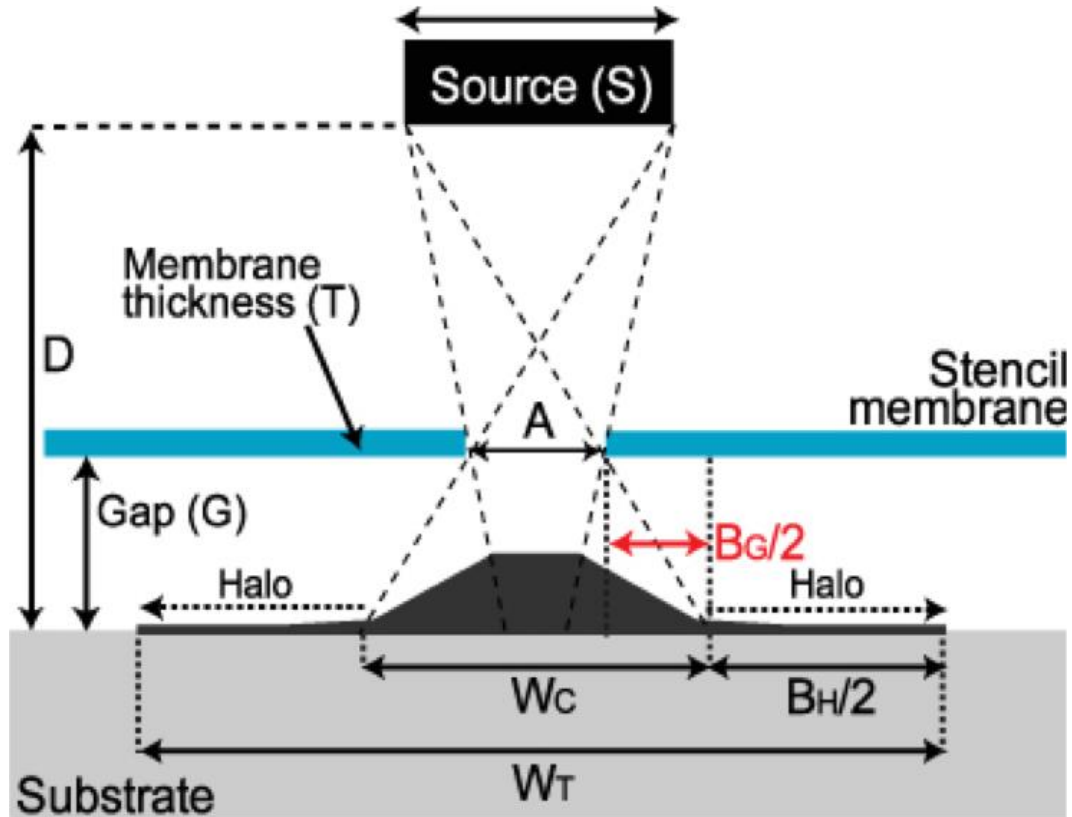
Blurring



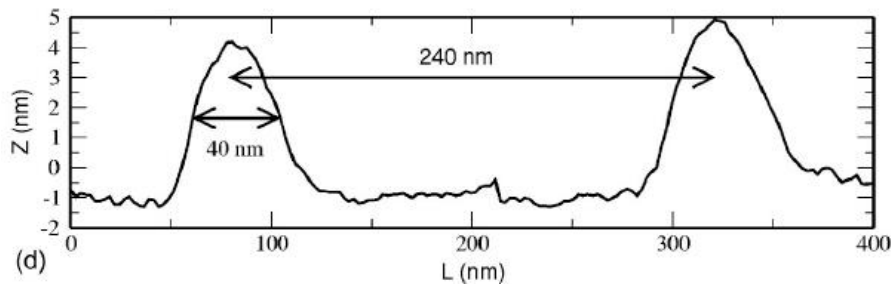
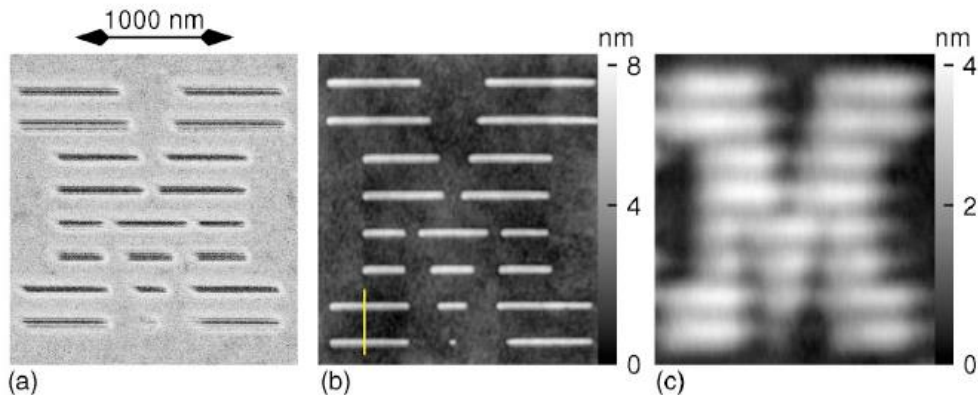
Alignment



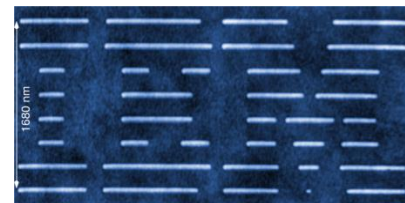
Stencil litho details



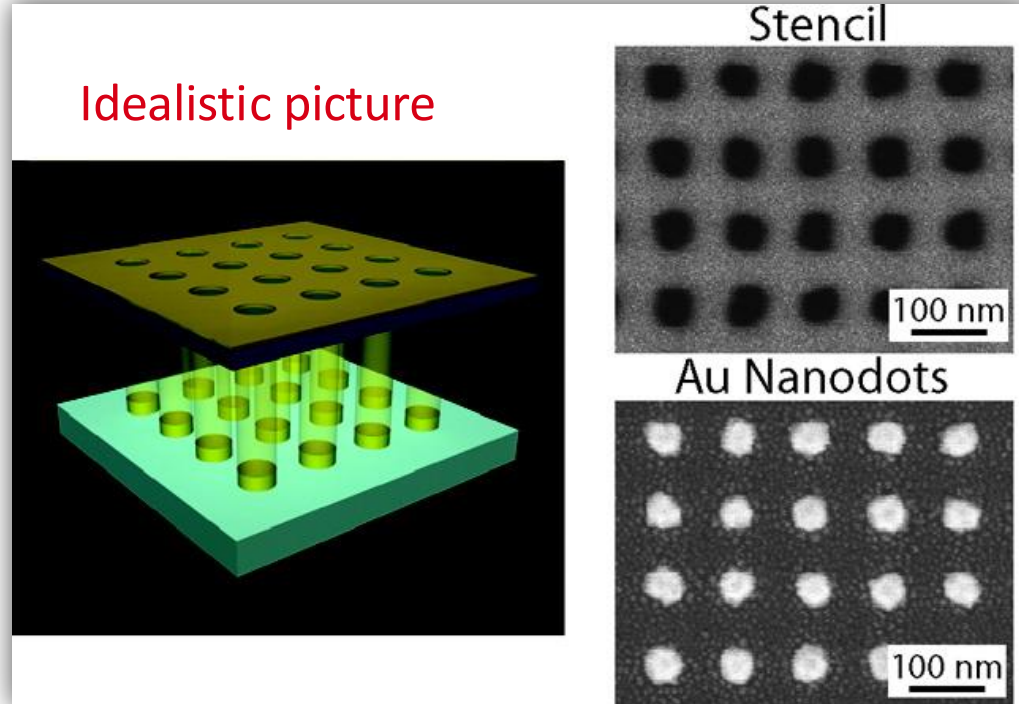
Watch out for surface diffusion



- (a) FIB image of the stencil mask used here
- (b) DFM image of the 40 nm wide Cu structure on SiO₂
- (c) DFM image of the C₆₀ structure (diffusion induced halo).
- (d) Line profile of the section marked.



Metallic nanostructures stenciled



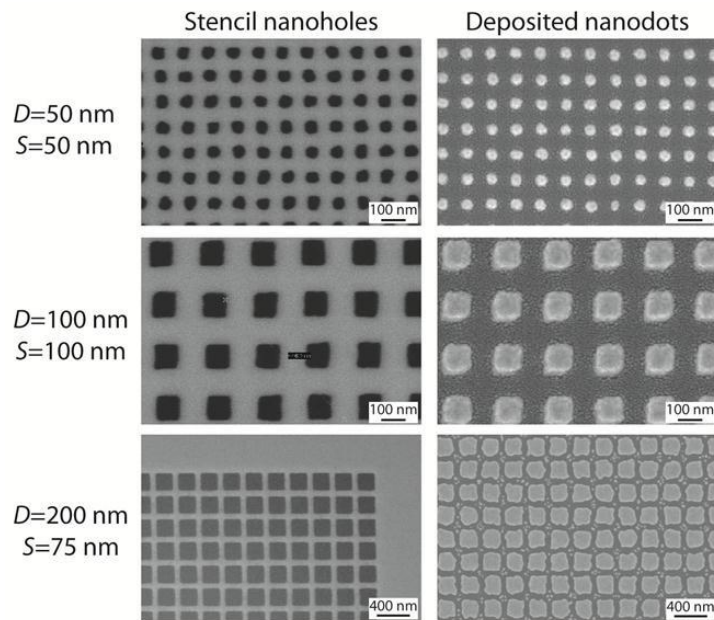
Reality
Blurring
Diffusion

5 nm Ti / 50 nm Au

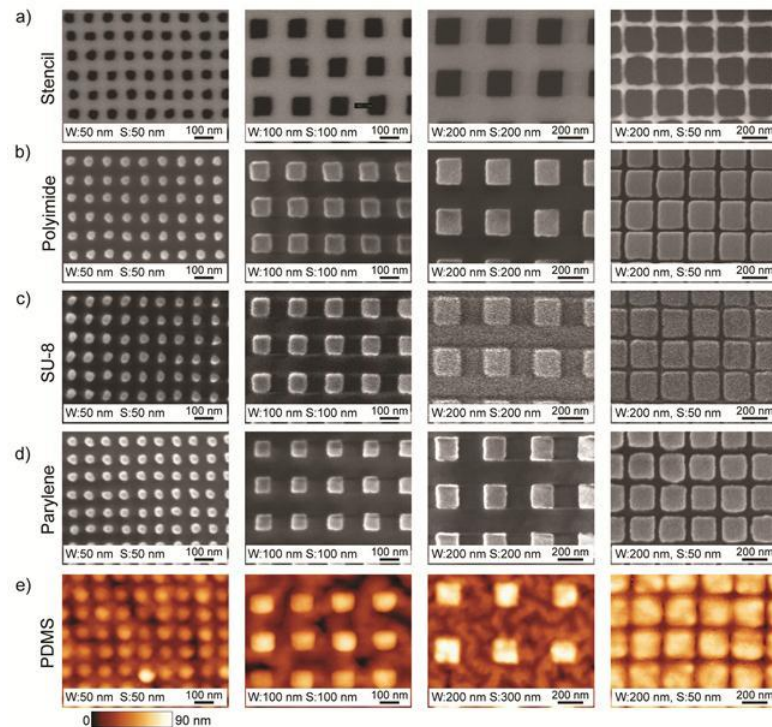
Metallic nanostructures stenciled onto ...

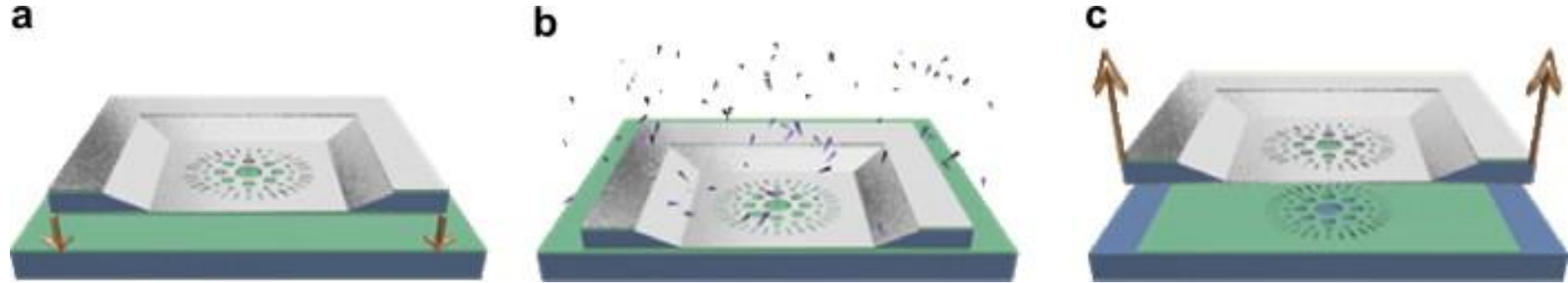
5 nm Ti / 50 nm Au

... **silicon** (Au clusters)

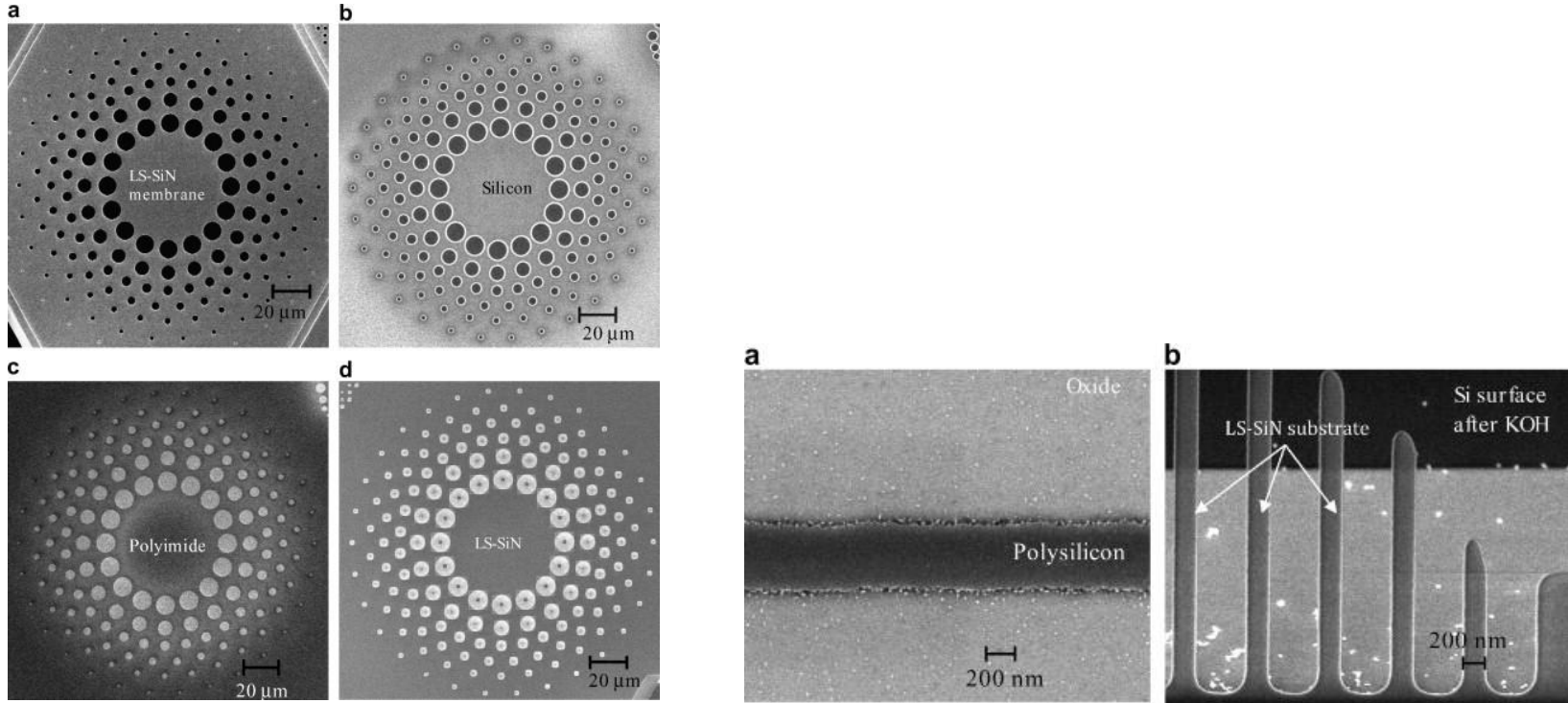


... **polymer** (no Au clusters)



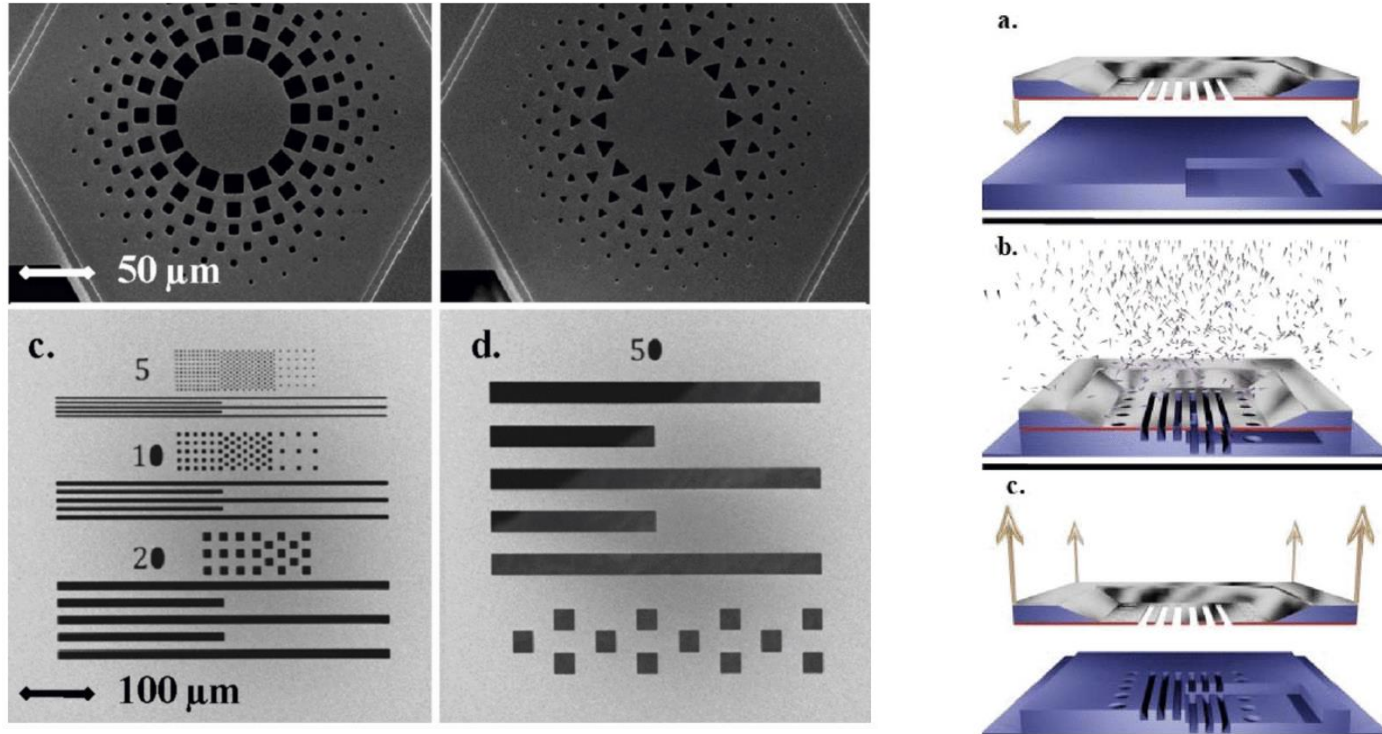


G. Villanueva, et al. Etching of sub-micrometer structures through Stencil, Microelectronic Engineering (2008)



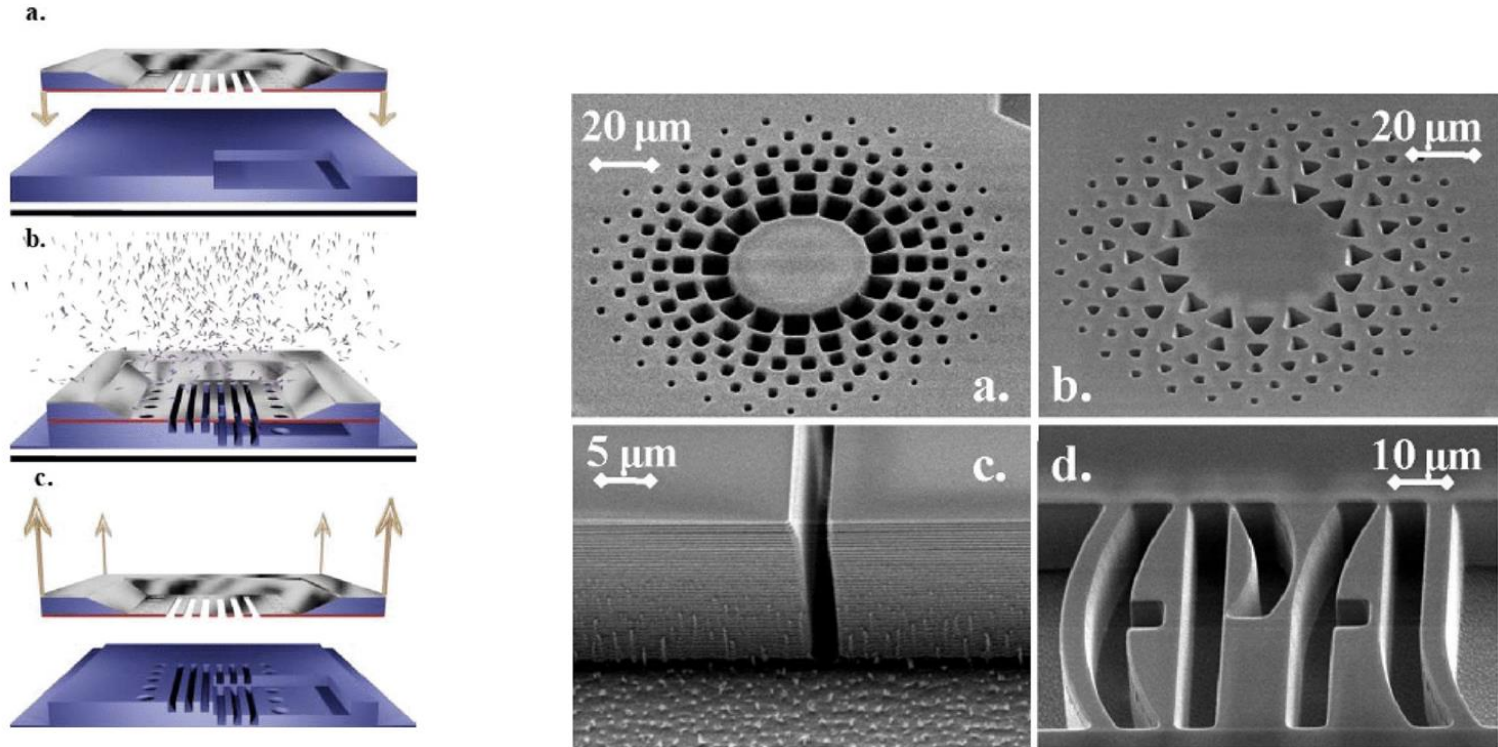
G. Villanueva, et al. Etching of sub-micrometer structures through Stencil,
Microelectronic Engineering (2008)

Deep Etching through stencils



G. Villanueva, O. Vazquez-Mena, C. Hibert and J. Brugger, "Direct Etching of High Aspect Ratio Structures Through a Stencil," 2009 IEEE MEMS conference

Deep Etching through stencils



G. Villanueva, O. Vazquez-Mena, C. Hibert and J. Brugger, "Direct Etching of High Aspect Ratio Structures Through a Stencil," 2009 IEEE MEMS conference

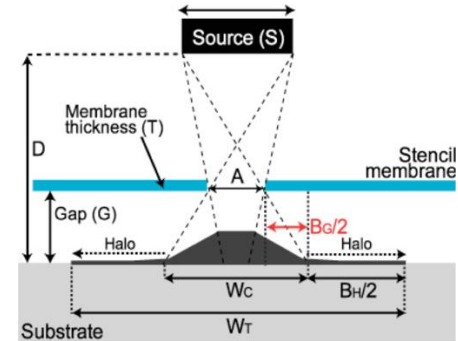
What else as local surface patterning method could be done through nanostencils?

- Deposition (PVD)
- Dry etching
- ...

Nanostencil problem: "forbidden" topology of closed loop patterns

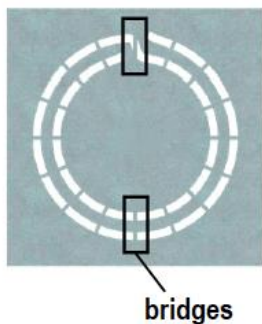


Add bridges &
make use of blurring

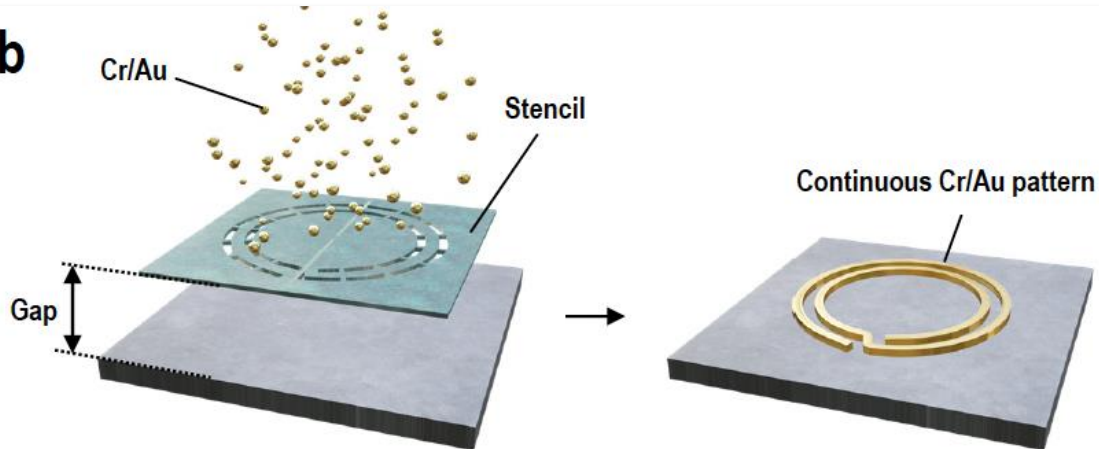


Bridge nanostencil: Split ring resonator on flexible substrate

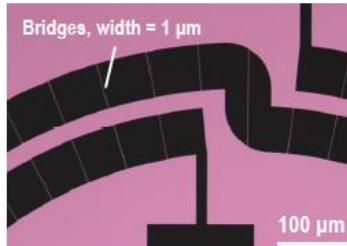
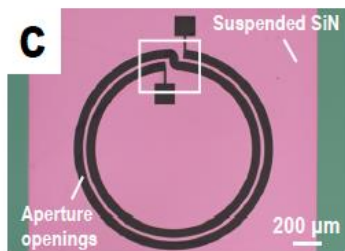
a Spiral structures



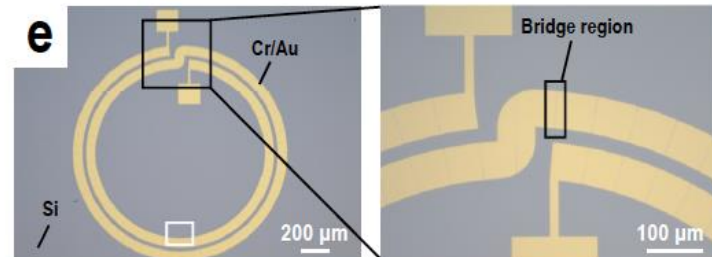
b

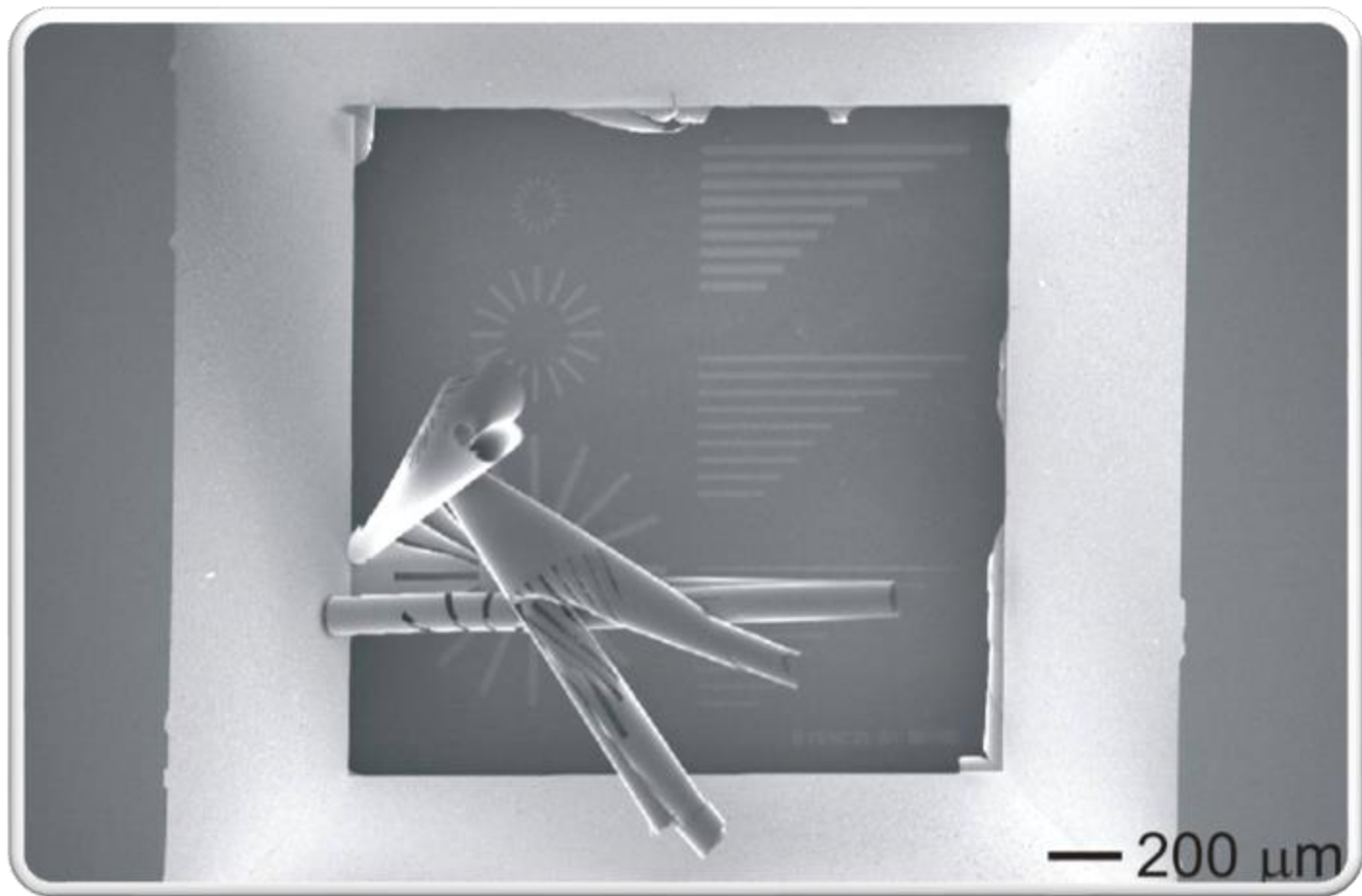


c



e

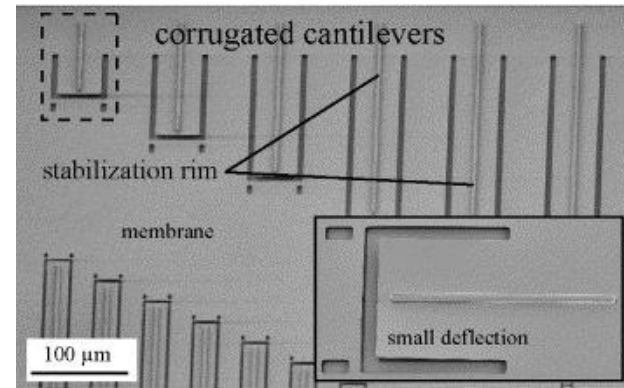
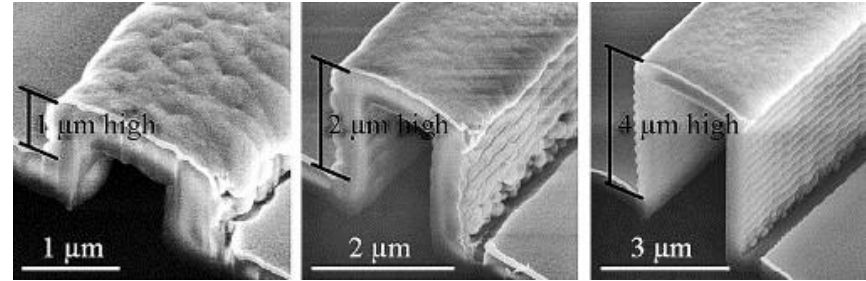
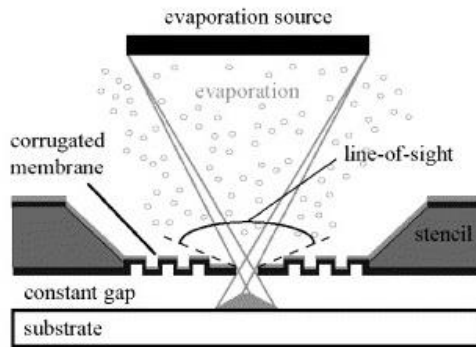
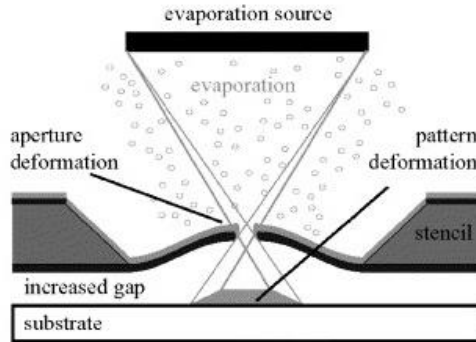




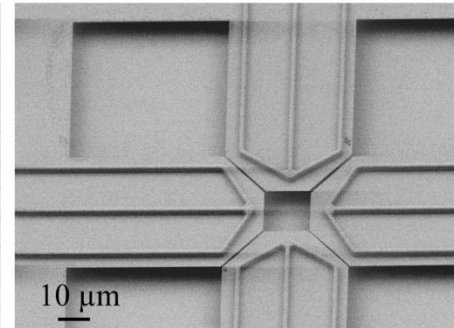
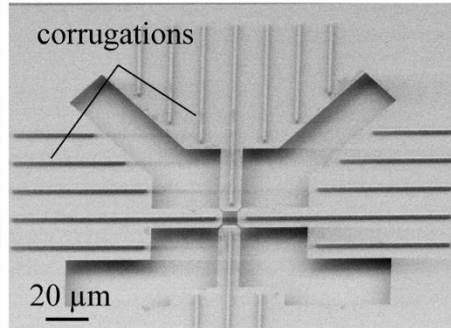
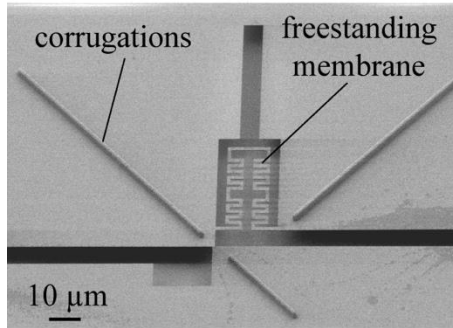
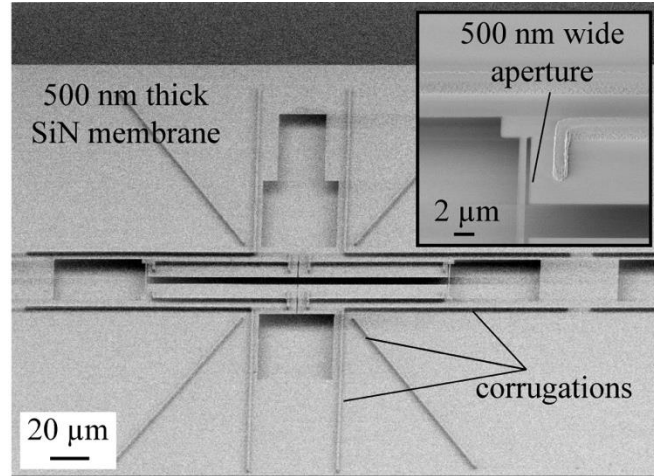
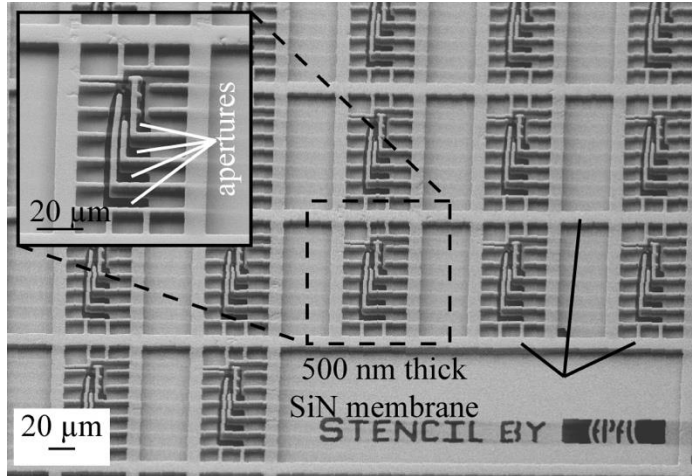
— 200 μm

— 500 μm

Solution to problem: increasing the moment of inertia by corrugation



M.A.F van den Boogaart et al., Sensors and Actuators A: Physical (2006)
Transducers 2005, Seoul



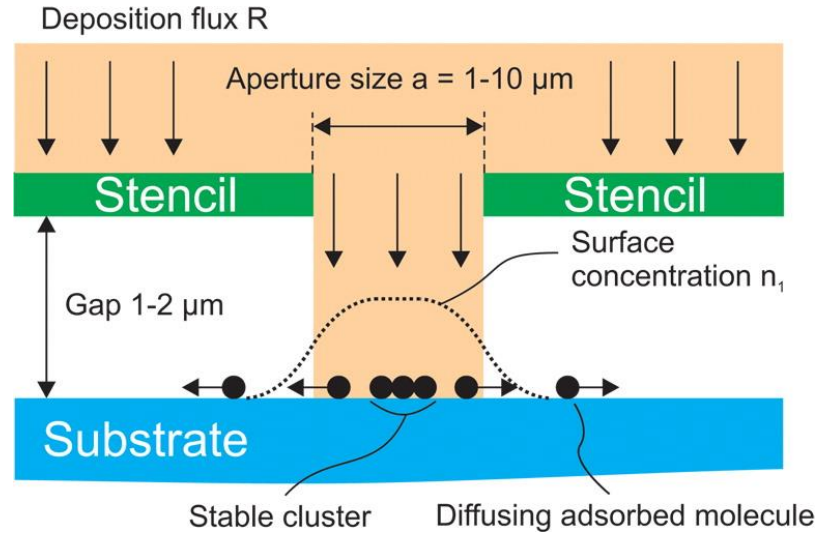
■

Hammer ('70s)

■

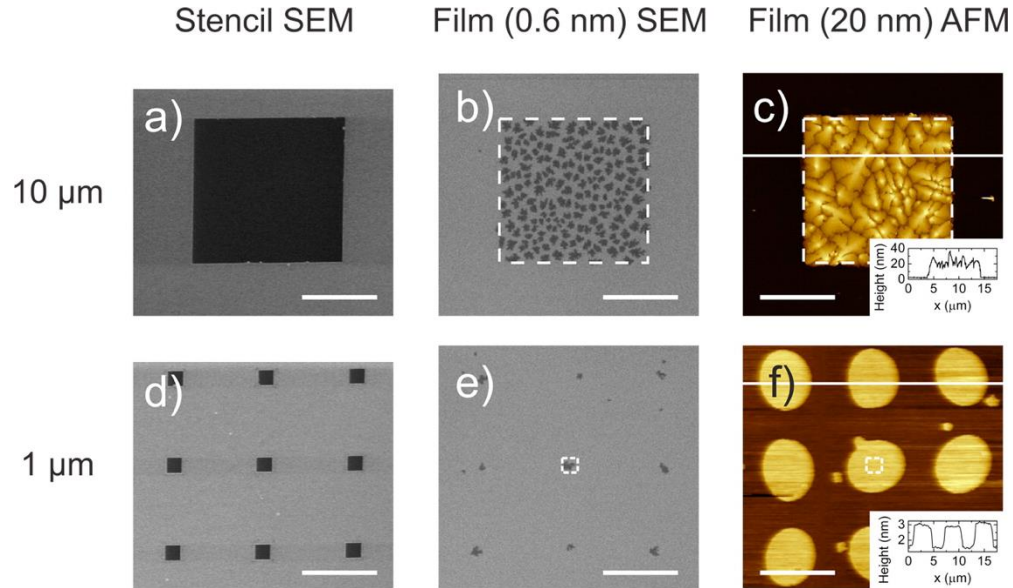
Van den Boogaart et al. 2008

Arrays of Pentacene Large Single Crystals by Stencil Evaporation

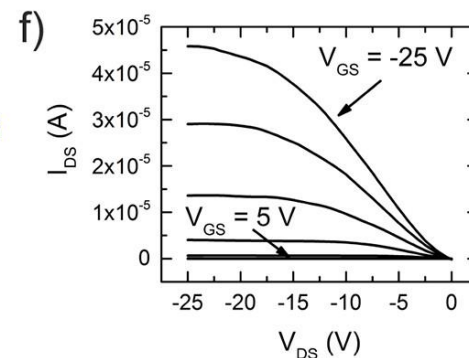
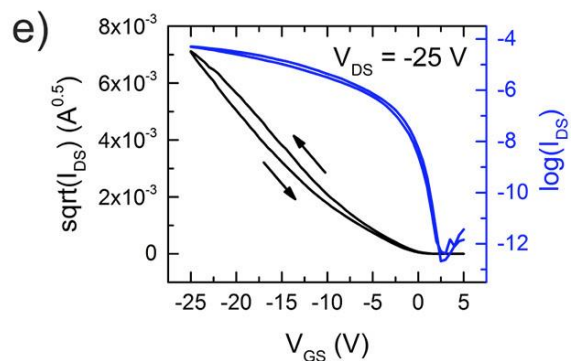
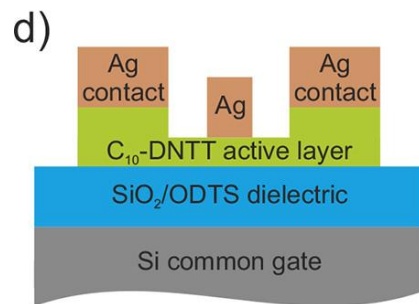
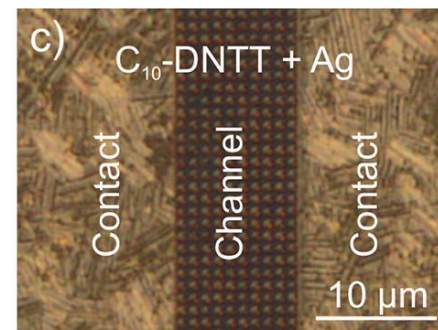
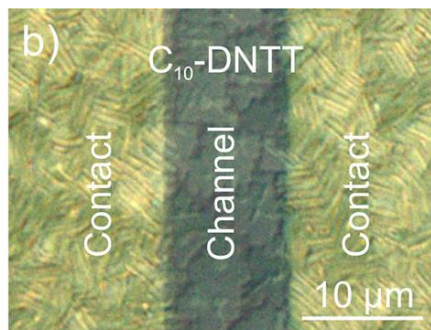
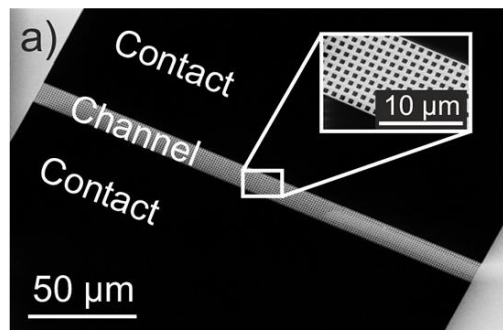


Arrays of pentacene single crystals
 Patterned on SiO_2 substrates
 through stencil evaporation
 Micron-scale apertures enables a
 control over nucleation and
 subsequent diffusive growth

Arrays of Pentacene Large Single Crystals by Stencil Evaporation



Depositing both, organic molecules and metal electrodes



F. VROEGINDEWEIJ^{1,✉}
E.A. SPEETS¹
J.A.J. STEEN²
J. BRUGGER²
D.H.A. BLANK¹

Exploring microstencils for sub-micron patterning using pulsed laser deposition

¹ University of Twente and MESA⁺ Institute for Nanotechnology, Faculty of Science & Technology, P.O. Box 217, 7500 AE Enschede, The Netherlands

² Microsystems Laboratory, Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland

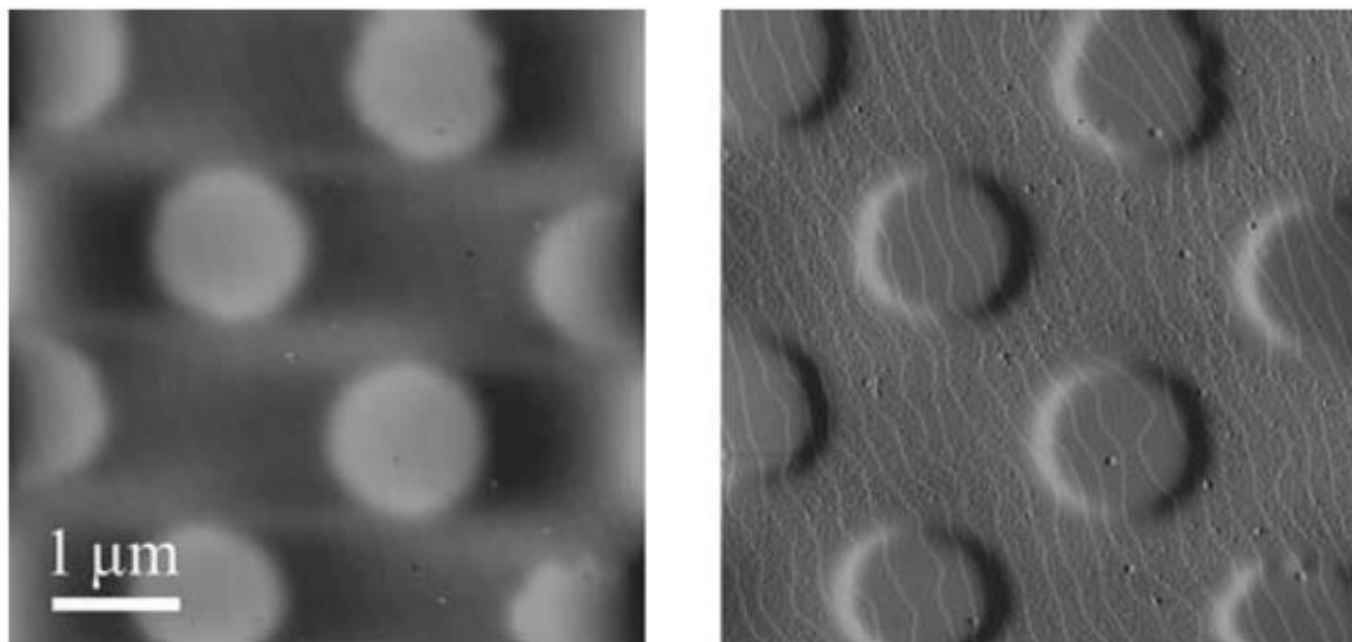
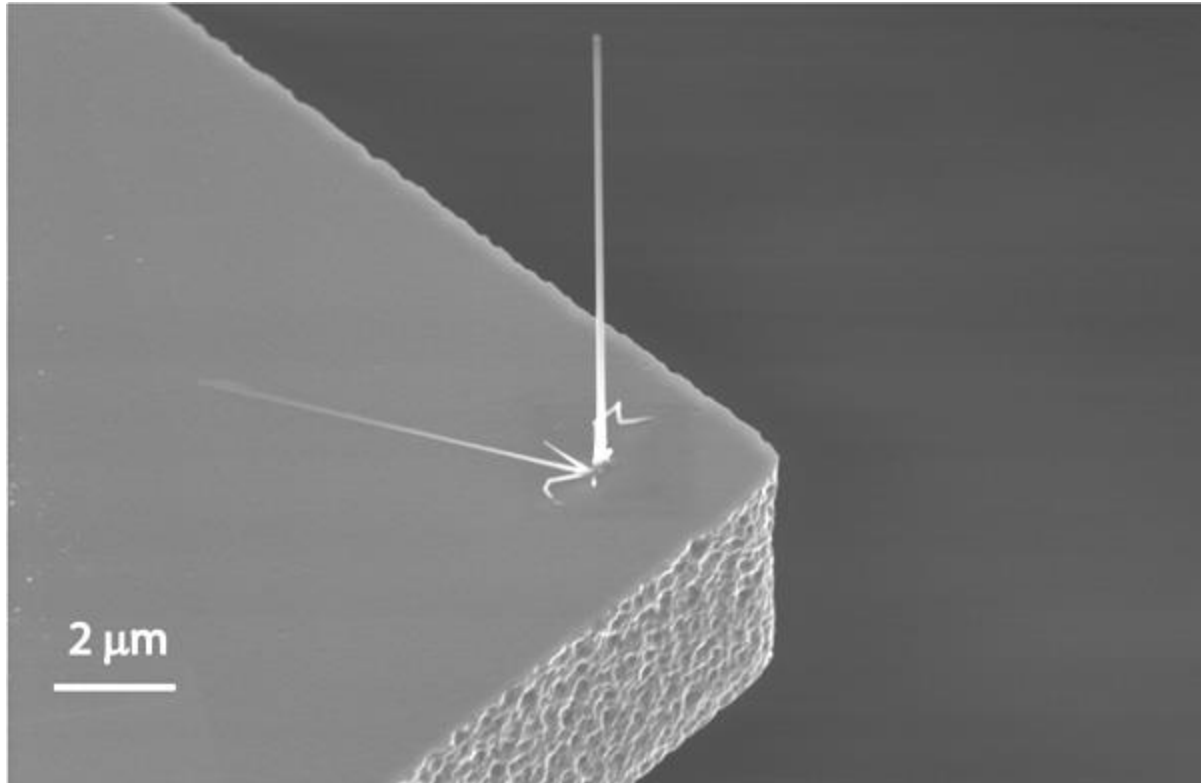
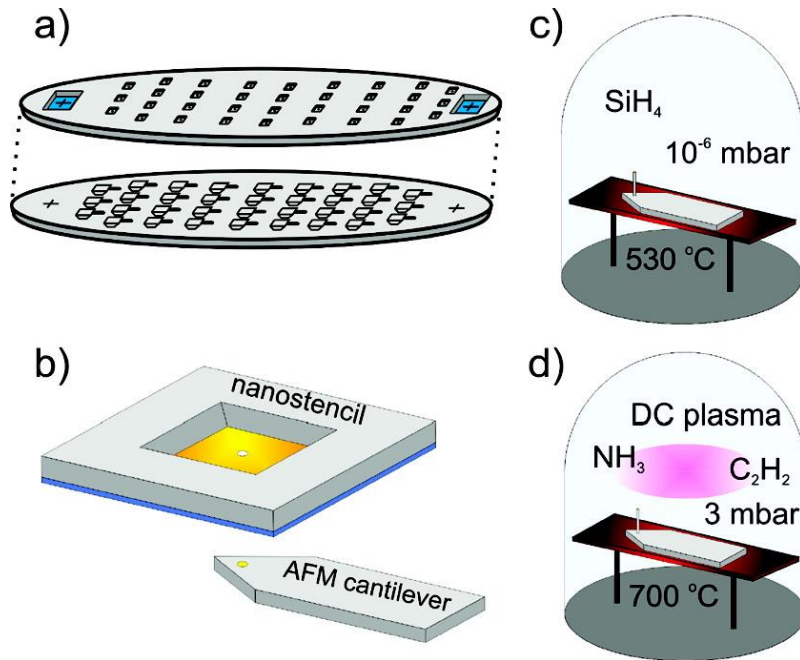


FIGURE 2 $5 \times 5 \mu\text{m}^2$ CM-AFM image of 5.2-nm-high Ni islands on a SrTiO_3 substrate. Height (*left*) and deflection (*right*) images. The deposition parameters used are a 5.0 J cm^{-2} fluence, 4.0×10^{-4} mbar Ar pressure, 2.5 ml min^{-1} Ar flow and a 42.0 mm target–substrate distance



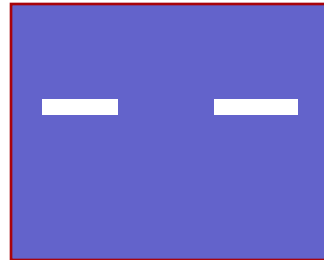
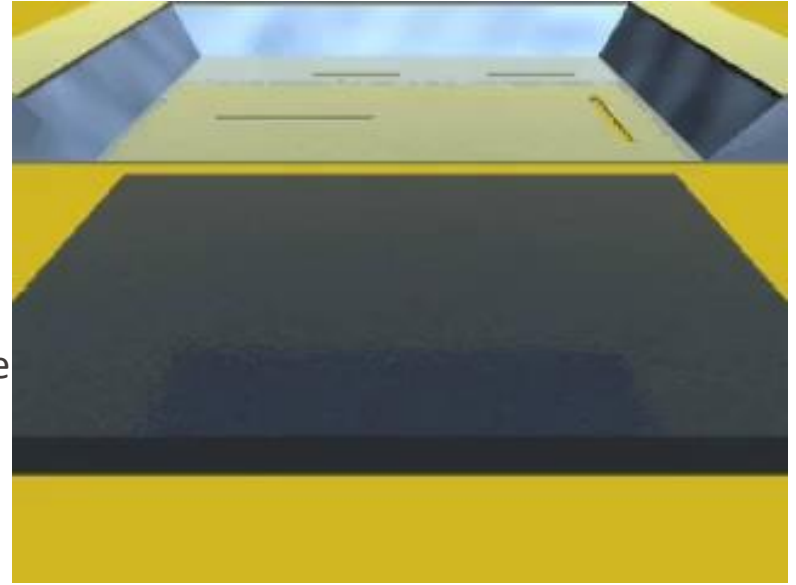
Stenciling on free-standing substrates

- Stencil fabrication for catalyst deposition
- Stencil alignment to cantilever full-wafer
- Catalyst deposition through aligned stencil
- CNT/Si NW growth
- AFM measurements

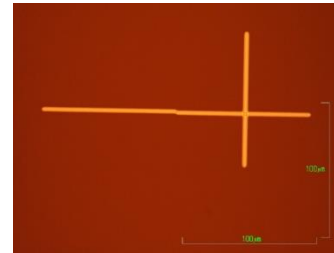


The moving shadow mask

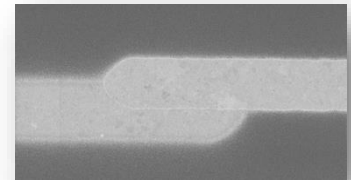
- Step and repeat
- Reposition stencil in vacuum between subsequent deposition steps
- No exposure to atmosphere
- In-situ oxidation
- Clean surface/interface
- Tunnel junctions
- 2 materials (or more)



stencil



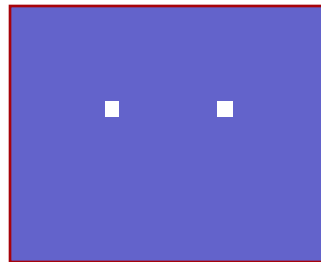
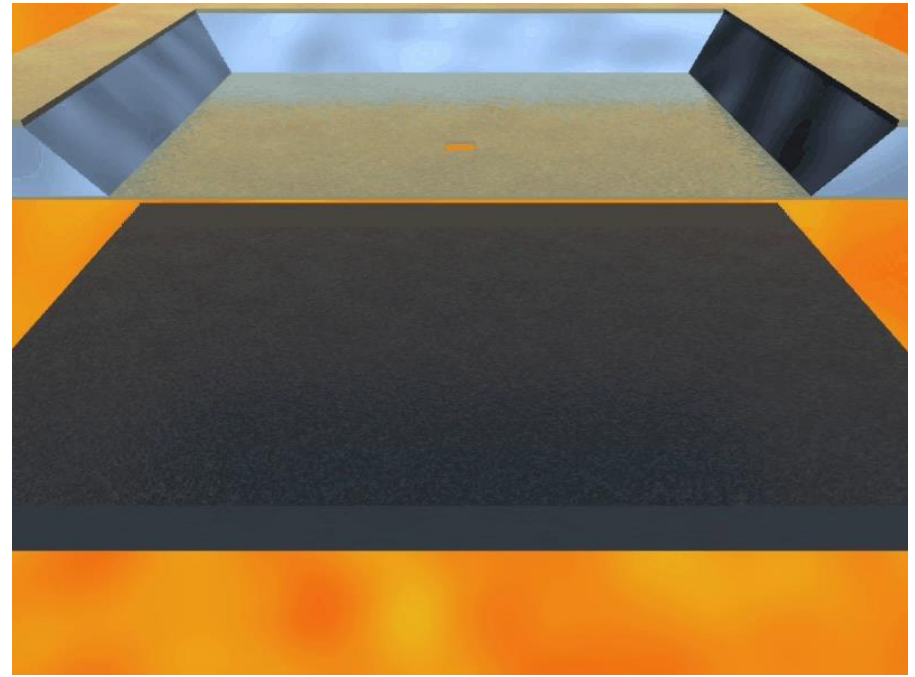
stitched



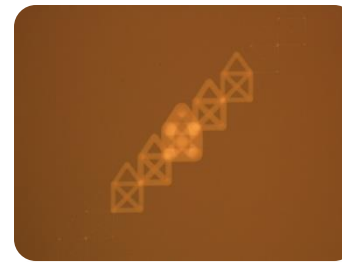
junctions

Dynamic stenciling

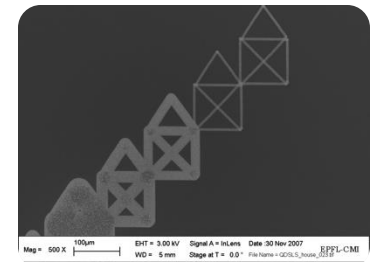
- Dynamic stencil
- Free motion in vacuum
- Rapid prototyping
- Flexible lithography
- PC controlled
- Parallel patterning
- Tapered film thickness



stencil

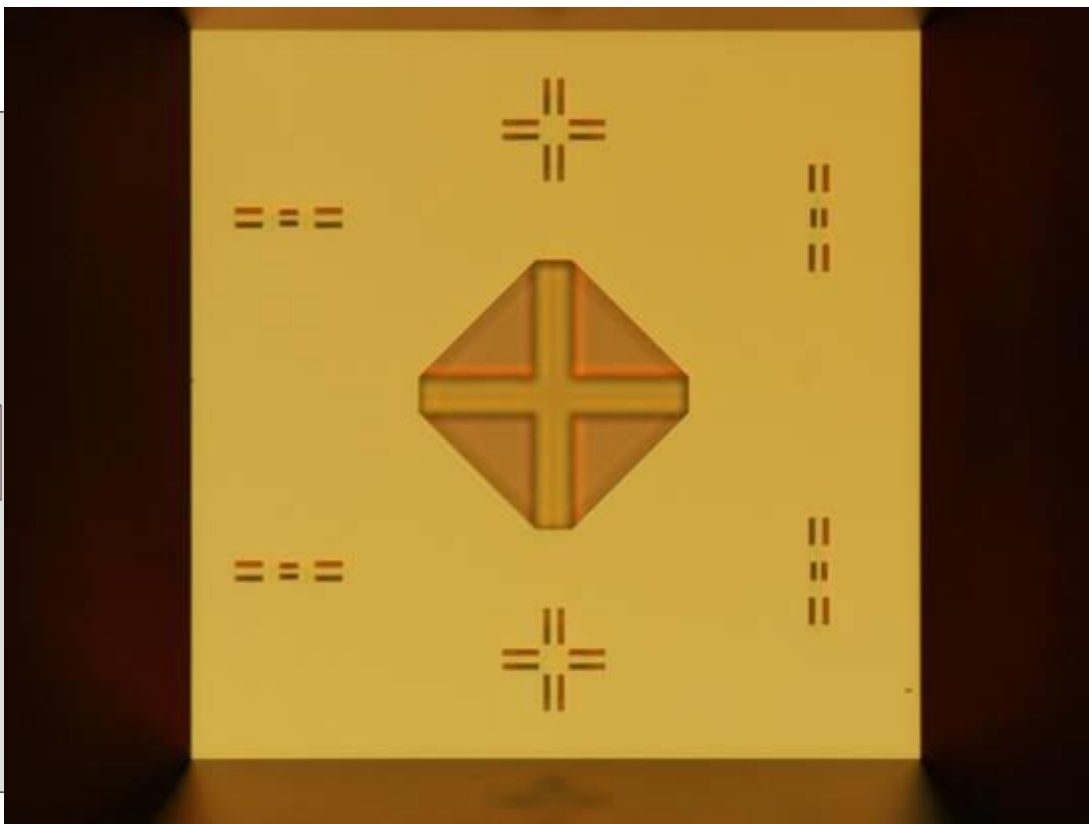
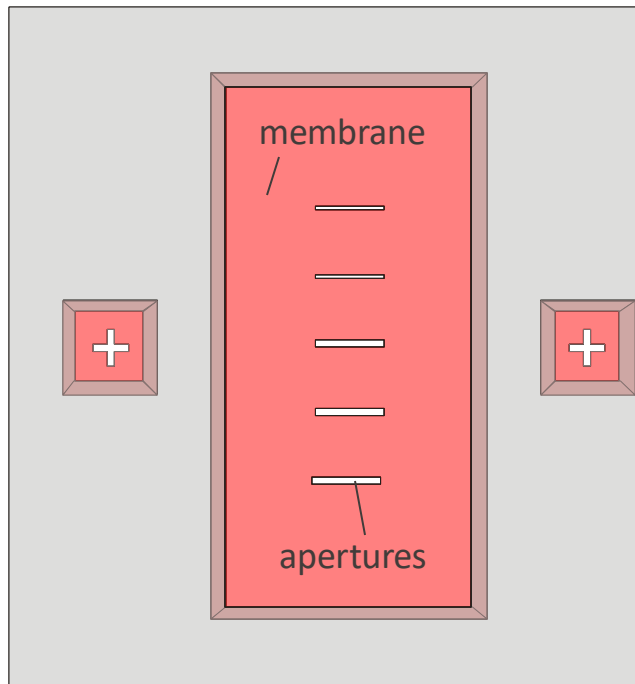


Free motion

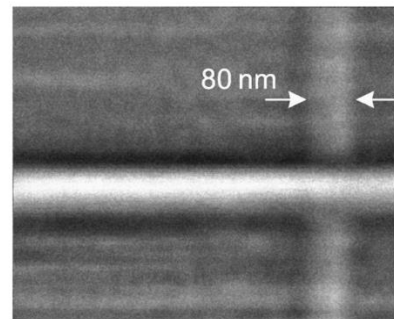
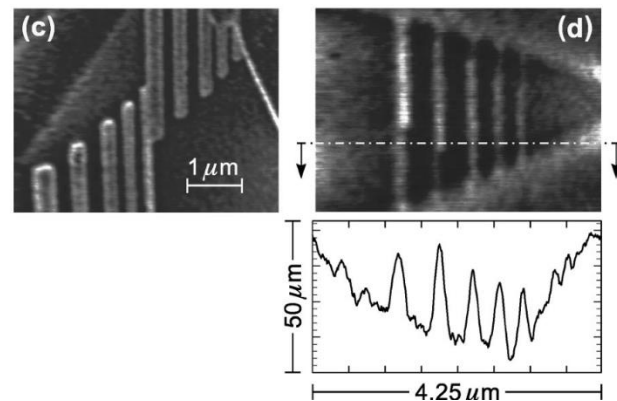
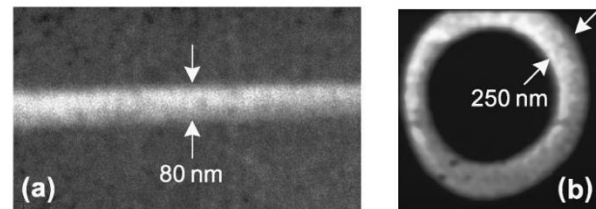
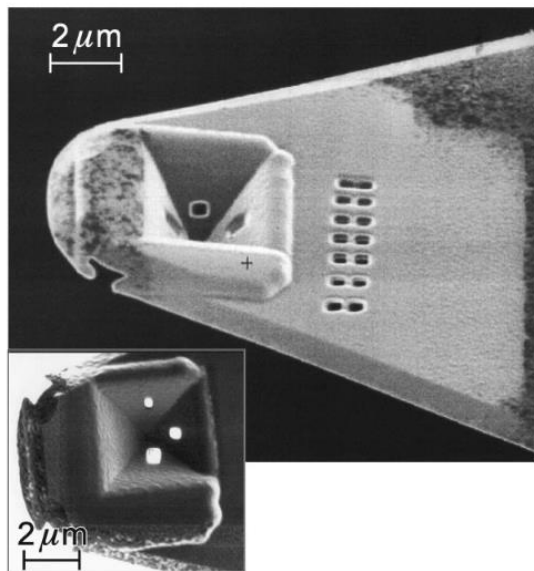
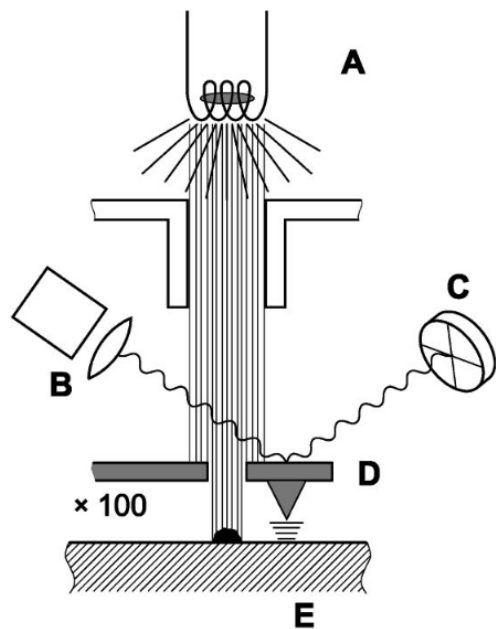


SEM image

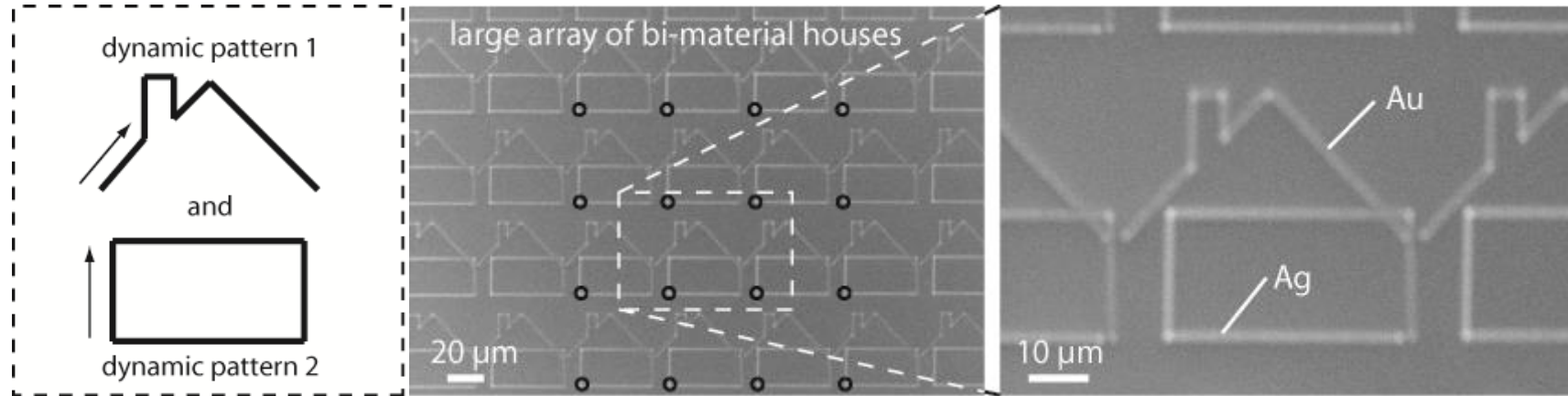
Nanostencil

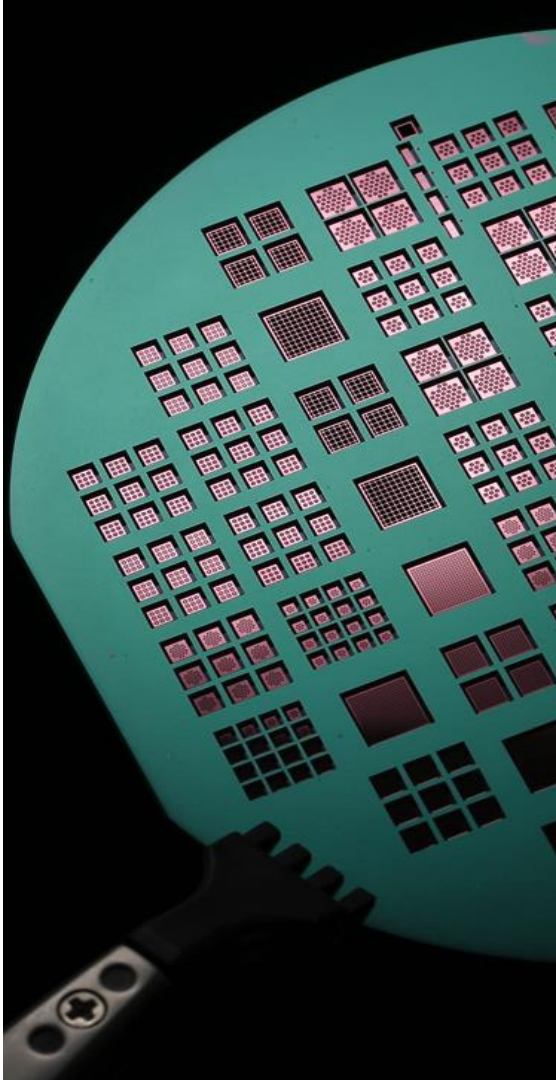


Dynamic nanostencil



Dynamic stenciling





Take away message Nanostencil

- Scalable to < 50 nm resolution
- Full wafer
- Vacuum clean
- No contamination of fragile materials
- Metal and organic materials, dielectrics

- Fine tuning of material flux
- Control crystal growth
- Micro-manufacturing of OE, flexible wearables, etc.